Notice of Allowability	Application No.	Applicant(s)	
	10/754,550	CHO, JANG-HO	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *request for continued examination and amendment received 01/22/2007*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *04/13/2007* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Linus Y. Park on 04/13/2007.

The application has been amended as follows:

Claim 1 (Twice Amended) A multi-threaded processor, comprising:

a processing pipeline including a number of stages, each stage processing at least one instruction, each instruction belonging to one of a plurality of threads; and

a fetch unit forming one of the stages of the pipeline and determining from which of the plurality of threads to fetch an instruction for processing by the processing pipeline, the fetch unit receiving information from at least one other stage of the processing pipeline and determining a processing time of the processing pipeline occupied by each of the plurality of threads based on the received information, the fetch unit determining from which of the plurality of threads to fetch [[an]] the instruction for processing by the processing pipeline based on the determined processing time for each of the plurality of threads, wherein the fetch unit generates a weighted instruction count for each of the plurality of threads, the weighted instruction count for each of the plurality of threads is a count of [[the]] instructions for each of the plurality of threads

~~with each instruction~~ weighted by cycle counts associated with processing the instructions for each of the plurality of threads.

Claim 2 (Twice Amended) The processor of claim 1, wherein the fetch unit determines a smallest determined processing time thread as [[the]] a thread from the plurality of ~~treads~~ threads from which to fetch an instruction for processing.

Claim 6 (Twice Amended) The processor of claim 5, wherein the fetch unit determines a thread associated with [[the]] a counter having a smallest count value as [[the]] a thread from which to fetch the instruction for processing.

Claim 9 (Currently Amended) The processor of claim 8, wherein the fetch unit determines [[the]] a thread associated with [[the]] a counter having a smallest count value as [[the]] a thread from which to fetch an instruction for processing.

Claim 10 (Currently Amended) The processor of claim 1, wherein the processing pipeline comprises:

an instruction decoder decoding instructions, which the fetch unit determines to fetch, to generate at least an operation type of [[the]] an instruction as decoder information; and

a queue storing [[the]] decoded instructions and issuing the decoded instructions to an execution unit for execution.

Claim 12 (Currently Amended) The processor of claim 1, wherein the processing pipeline further comprises:

an instruction cache storing instructions, and outputting an instruction to [[the]] an instruction decoder based on which instruction the fetch unit determines to fetch; and

an address renamer mapping a logical address generated by the instruction decoder for an instruction into a real address of a memory device in an execution unit.

Claim 13 (Twice Amended) A method of fetching instructions for processing in a multi-threaded processor, comprising:

receiving, at a fetch unit of a processing pipeline, information from at least one other stage of the processing pipeline, the processing pipeline including a number of stages, each stage processing at least one instruction, each instruction belonging to one of a plurality of threads;

first determining a processing time of the processing pipeline occupied by each of the plurality of threads based on the received information by generating a weighted instruction count for each of the plurality of threads as the determined processing time of each of the plurality of threads, the weighted instruction count for each of the plurality of threads is a count of [[the]] instructions for each of the plurality of threads ~~with each instruction~~ weighted by [[the]] cycle counts associated with processing ~~the instruction~~ the instructions for each of the plurality of threads; [[and]]

second determining from which of the plurality of threads to fetch an instruction for processing by the processing pipeline based on the determined processing time for each of the plurality of threads; and

fetching an instruction for processing by the processing pipeline based on said second determining.

Claim 14 (Twice Amended) The method of claim 13, wherein the second determining step determines a thread having [[the]] a smallest determined processing time as [[the]] a thread from which to fetch an instruction for processing.

Claim 16 (Currently Amended) The method of claim 15, wherein the received information further includes the operation type of ~~instruction~~ instructions leaving the processing pipeline.

Claim 18 (Currently Amended) The method of claim 17, wherein the second determining step determines [[the]] a thread associated with [[the]] a counter having a smallest count value as [[the]] a thread from which to fetch an instruction for processing.

Claim 20 (Twice Amended) The method of claim 19, wherein the first determining step comprises:

incrementing, for each of the plurality of threads, a counter associated with each of the plurality of threads by [[the]] cycle counts associated with each instruction of the associated thread in the processing pipeline; and

decrementing, for each of the plurality of threads, the counter associated with each of the plurality of threads by the cycle counts associated with each instruction of the associated thread leaving the processing pipeline.

Claim 21 (Currently Amended) The method of claim 20, wherein the second determining step determines [[the]] a thread associated with [[the]] a counter having a smallest count value as [[the]] a thread from which to fetch an instruction for processing.

Statement of Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

The prior art of record including the disclosures of Emer et al. (U.S. Patent No. 6,073,159), Cota-Robles (U.S. Patent No. 6,658,447), Borkenhagen et al. (U.S. Patent No. 6,076,157), Tullsen et al. ("Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreading Processor"), Luo et al. ("Balancing Throughput and Fairness in SMT Processors"), and El-Moursy et al. ("Front-End Policies for Improved Issue Efficiency in SMT Processors") neither anticipates nor renders obvious the following limitations of claim 1 (in combination with all other features in the claim):

"wherein the fetch unit generates a weighted instruction count for each of the plurality of threads, the weighted instruction count for each of the plurality of threads is a count of instructions for each of the plurality of threads weighted by cycle counts associated with processing the instructions for each of the plurality of threads".

Claims 2-12 depend from claim 1 and are considered allowable for at least the reasons noted above with respect to claim 1.

The prior art of record including the disclosures cited above neither anticipates nor renders obvious the following limitations of claim 13 (in combination with all other features in the claim):

"first determining a processing time of the processing pipeline occupied by each of the plurality of threads based on the received information by generating a weighted instruction count for each of the plurality of threads as the determined processing time of each of the plurality of threads, the weighted instruction count for each of the plurality of threads is a count of instructions for each of the plurality of threads weighted by cycle counts associated with processing the instructions for each of the plurality of threads"

Claims 14-21 depend from claim 13 and are considered allowable for at least the reasons noted above with respect to claim 13.

The Examiner notes that "cycle counts", as noted by the applicant in the remarks filed 01/22/2007, are defined in the applicant's specification to "refer to cycle count values of system clocks used by at least one of the instruction decoder 130, the register renamer 140, and the instruction queue unit 150, as non-limiting examples in processing the instruction" (paragraph [0024]).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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DONALD SPARKS
SUPERVISORY PATENT EXAMINER